IJRD International Journal of Research & Development Organisation

ISSN-4567-7860

JOURNAL OF ELECTRICAL AND ELECTRONINS ENGINEERING

Interleaving Test Algorithm for Detecting Defects in DRAM

Anitha K,
Department of Electronics and Cmmunication Engineering,
Bannari Amman Institute of Technology,
Sathyamangalam.

Sampath P,
Department of Electronics and Communication Engineering,
Bannari Amman Institute of Technology,
Sathyamangalam.

***Abstract*—Since the minimum feature size of dynamic RAM has been down-scaled. Several studies have been carried out to determine ways to protect cell data from leakage current in many areas. In the field of testing, more appropriate test algorithms are required to detect weak cells with leakage-current sources. In this paper, we propose an interleaving test algorithm that takes into account the equal bit-line stress regardless of the cell location. The proposed test algorithm allows screening of weak cells and correct it due to the subthreshold leakage current.**

***Index Terms*—Bit-line stress time, maximum stress time, sub threshold leakage-current defect, test algorithm**.

I INTRODUCTION

More than four decades, the simple structure of the dynamic RAM (DRAM) cell and continuous improvement in lithography and dry-etching technology has made DRAM grow exponentially in a large-scale integration and has decreased the minimum feature size in memory chips. For better performance and lower power consumption, the memorychip has been scaled down everyyear. The 2010ITRS roadmap reports that the minimum feature size of DRAM will be 20 nm in 2017 and 10 nm in 2023. However, with this down-scaling trend of the minimum feature size and power, many problems (capacitor/word-line/bit-line bridges, coupling noise, P-MOS/N-MOS ratio, and leakagecurrent and so on) need to be considered. Furthermore, due to the demands of higher density and speed, the leakage-current problem has recently become more serious. With the short length of the word-line channel, the sub threshold leakage current will increase more. To prevent this sub threshold leakage-current problem, channel doping should be increased in order to maintain adequate control of short-channel effects. However, junction leakage current due to band-to-band tunneling and gate-induced drain leakage current may increase as a result of high channel doping.

The variability of the threshold voltage can also increase due to defects resulting from manufacturing aberrations. To detect these complicated defects, it is necessary to analyze the fail mechanism and find appropriate test algorithms. Conventional DRAM testing can be grouped into retention testing and functional testing. Retention testing is a test method that screens leakage-current defects by operating read and write functions containing a particular delay time. In functional testing, March elements that are a finite sequenceof read or write operations applied to a cell in memory before proceeding to the next cell are conducted on each memory cell in order to detect the cell-to-cell bridge and coupling noise. Due to the flexibility of these March elements, most built-in self-test (BIST) architectures adopt functional test algorithms using the conventional March elements but with the downscaling of the device, conventional March testing cannot properly detect the leakage-current defects, and these defects have to be assessed using the time-consuming stress method. To test for leakage-current defects, several studies have attempted to implement retention testing using special techniques. The word-line-pulsing technique has been proposed as a means of detecting weak cells by coupling nearby neighbor word lines. This technique results in an adjustable test stress based on setting the word-line enable time. This methodcan be used to detect sub threshold leakage-current defects; but when it is used in DRAM, it has to considerstress equality according to the cell location during the stress enable time. March complex read faults (CRF, which is also suggested in static RAM) detects faulty cells induced by the leakage current using the voltage gap between the bit line and the target cell with opposite data. However, according to our experimental results, March CRF has lower screenability than the wordline pulsing technique. X-direction-Extended March C- and Y-direction MATS are proposed to screen retention faults using self-refresh and time delay in EDRAM, but these studies mainly deal with detecting retention faults and analyzing the relationship between the leakage current and temperature. They do not focus on the sub threshold leakage-current defects. A large VDS data retention test is also proposed to detect leakage-current defects in DRAM.

However, most of the previous works have

not considered stress differences among cells caused by cell locations due to the refresh operation of DRAM. Therefore, the quality problems can occur. Thus, a more powerful screening technique is needed to detect sub threshold leakage-current defects. This paper proposes a new efficient test algorithm for equal bit-line stress in order to screen for sub threshold leakagecurrent defects. During the stress time, the algorithm can detect other leakage-current defects. First, the leakage-current sources and scrambling technique are discussed, and then the proposed test algorithm operation is explained. This paper is organized as follows. Section II introduces the simplified DRAM architecture, which is an essential guide for determining the solution to equal bit-line stress. Sections III explain the new test algorithm and the simulation results. Finally, Section IV concludes the paper.

II BACKGROUND

A.Main Leakage-Current Sources

The gate-oxide thickness needs to be decreased to improve gate controllability and short-channel behavior, and the doping concentration needs to be increased to maintain the electric field; however, the smaller the device becomes,the more easily the leakage-current defects occur. In order to screen these leakage-current defects, primary leakage-current sources need to be classified and analyzed.Thereare several leakage-current sources that affect the retention time of the cell capacitor. The tunneling leakage current into and through the gate oxide occurs in proportion to the reduction of the gateoxide thickness, and sub threshold leakage current occurs with low sub threshold voltage due to the low concentration of the minority carrier and the decrease in gate width. P-mos N-mos (P-N) junction leakage current is caused by the high electric field of the depletion region. Generally, in order to find defects early and more easily, the worst operation environment must be induced. For example, voltage gap, delay time, repeated march operation, temperature, humidity, and other conditions can be applied. In this sense, cells that are weak due to the leakage current can be detected by increasing the voltage gap between the leakage-current sources in order to more easily accelerate the flow of leakage current at high temperatures. The tunneling leakage-current into and through the gate oxide can be detected by applying a high voltage to the gate while writing a low voltage to the cells. Subthreshold leakage-current and P-N junction-leakage current can also be detected using the high voltage difference between the drain and the source or body.

In addition to the voltage gap, the time delay is usually used to find weak cells that leak marginally at a certain time. This time-delay method lengthens the test time, but is necessary to guarantee device quality. Therefore, the proper time delay should be considered according to the customer's needs for satisfying the quality.

B. Basic Cell Array

The gates of the DRAM cells are tied to the row decoder, and the bit-line pairs are connected to the sense amplifier, as shown in Fig. 1. A sense amplifier is composed of a pair of cross-connected inverters between the bit lines. When the address and row access signal (RAS) instruction are loaded to the device, each row of the selected cells is active. In this operation, the data stored in the cells of the selected row address are amplified and stored again by the sense amplifiers. This operation of an RAS instruction to read or write is like the DRAM refresh operation, which is activated periodically to store the cell data. When the address and column access signal (CAS) instruction are transferred, the selected column cells of the activated row cells are accessed. Through these operations, the desired data can be read or written via the Din or Dout pin.

The bit-line pairs are connected in parallel to the sense amplifier to reduce the bit-line coupling noise. This array architecture is called the folded bit-line array. This array usually has a small feature size of 8F2 (F: feature size), and has proven to be the most reliable design. Another array scheme called the open bit-line array has smaller feature sizes (6F2 or 4F2) than the folded bit line.

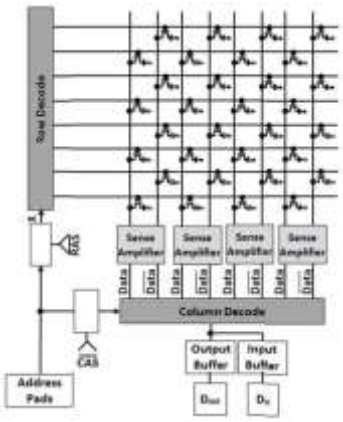


Fig. 1.Simplified DRAM diagram.

This scheme has high density and cell efficiency, and is also used when reducing the number of word lines to ease the impact of a bit-line interference noise on DRAM scaling. But there is no

difference in operating the DRAM cells between the folded bit line and open bit-line architecture. Therefore, the folded bit-line array architecture is used in this paper for better understanding.

C. Scrambling

The logical structure differs from the physical internal structure of the chip to optimize the memory layout more efficiently.Therefore, logically adjacent addresses may not be physically adjacent. This is called address scrambling.

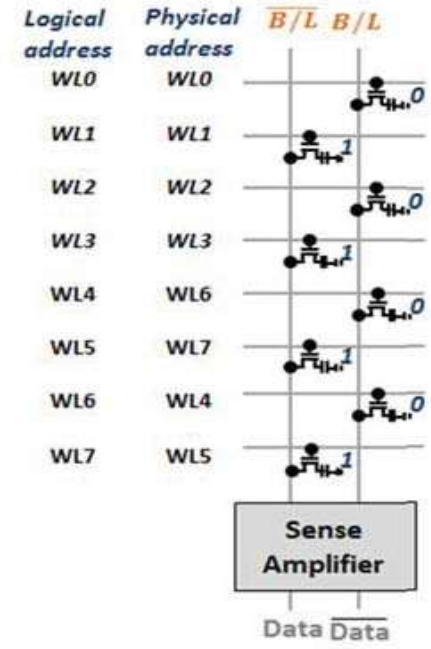


Fig. 2.Address and data scrambling.

Likewise, data scrambling means that logically adjacent data are not physically adjacent. Fig. 2 shows the twisted address line between the physical and logical addresses and the data status when the value of 0 is transferred to the cells without using scrambling scheme. In this case, the logical address of WL4, 5, 6, and 7 is different from the physical address due to the efficiency of the memory layout. And in case of the memory cell, which is based on the bit line, the inverted data are written into the cells connected to the bit bar line. When a test algorithm is implemented, different types of data backgrounds are used and Fig. 3 shows commonly used data backgrounds (DB), which are listed below.

1) Solid: All cells are filled with "0."

2) 1Row Bar: Alternating between "0" and "1," all cells are written in the row direction.

3)1ColumnBar:Alternatingbetween"0" and"1," all cells are written in the column direction.

4) 2Row Bar: Alternating between a pair of "0" and "1," all cells are written in the row direction.

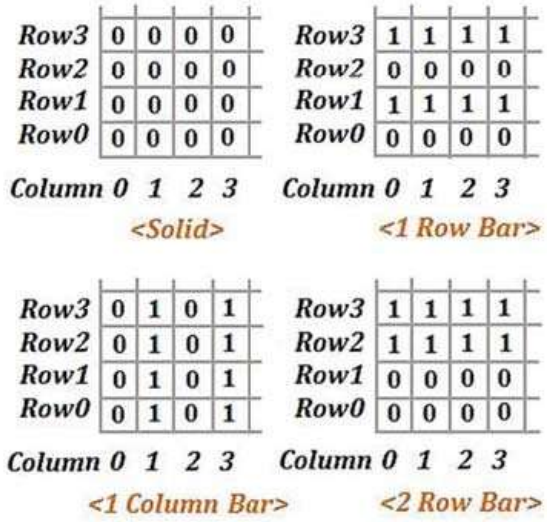


Fig. 3. Commonly used data background

It is necessary to write a proper background data for test algorithms. For example, when data value 0 is written to the cells, the 1-Row Bar data background is physically implemented. As mentioned previously, the inverted data are written into the cells connected to the bit bar line and the directed data are written into the cells connected to the bit line. But the Solid data background can be implemented by using the scrambling enabled scheme. When the scrambling enabled scheme is used, the scrambling scheme makes changed the data connected in the bit bar line to the inverted data. Therefore by using the scrambling-enabled scheme, the intended data of "0" can be written physically to the cells. In this paper, only data scrambling is considered for better understanding.

III PROPOSED NEW-TEST ALGORITHM

A. Concept

The concept of the proposed test algorithm is shown in Fig. 4. This simplified DRAM array is composed of eight rows and one column, and is implemented using a 2-Row Bar data background with scrambling enabled. Cells of word lines 0, 1, 4, and 5 are stored as "0," and cells of word lines2, 3, 6, and 7 are stored as "1." During the read operation of the first word line, the data stored as "0" is transferred to the bitline through the gate transistor. The sense amplifier then pulls down the bit line to "0" and pulls up the bit bar line to "1." When the first word line is activated at a specified time, the bit-line

cells stored as "1" are stressed during the activated time because of the voltage difference between the cell data and the voltage level of the bit line. The stress of the cells stored at the same voltage level as the bit line can be ignored because that stress is very small compared with that of cells stored at a different voltage level. Cells stored as "0" data at the bit bar line are also stressed by the voltage difference with the bit bar line.

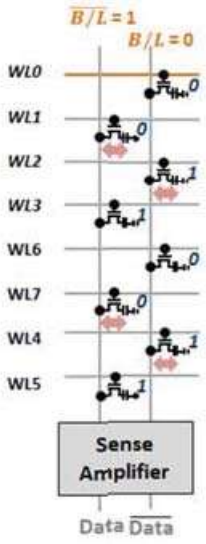


Fig. 4.Concept of the proposed test algorithm.

If the first word line is activated more than a certain number of times, then the cells stored as opposite data with the bit line and bit bar line are stressed during the activated time. If cells have a defect caused by the threshold leakage-current, the defect-cell data are easily changed to the opposite value during the stress time. Furthermore, these defects can be detected by setting an appropriate activated time of the word line depending on screenability in order to optimize the test conditions.

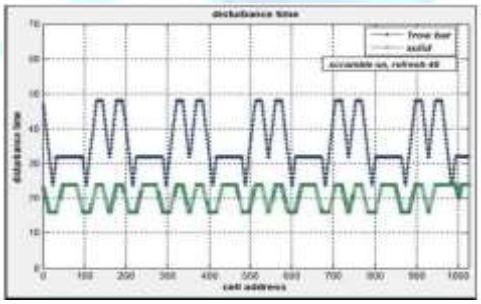
B. Statistical Analysis Model

In order to estimate the stressability of memory cells, it is necessary to calculate the stress intensity using a mathematical expression. When a word line is selected, the selected cell data (Dk) is transferred to the sense amplifier through the bit lines or bit bar lines. The sense amplifier then pulls the bit line or bit bar line to the data level of the selected cell. During the activated time of the word line k, the cell i receives the stress that causes the subthreshold leakage-current. Thus, the maximum stress time (MSTi) of cell i can be defined as follows:

$$MST_i = Maximum\left\{\sum_{k=0}^{i-1} S_k R_t, \sum_{k=i+1}^{N-1} S_k R_t\right\}$$

Where Sk indicates the stress effect of each cell k, Rt is the read time when the word line of cell k is activated, and N is the number of word lines per sense amplifier. If the stored cell data of i differs from the bit line or bit bar line transferred from the activated cell data k (Di ≠Dk), then the stress effect is available. Thus, the stress effect of Sk can be expressed as 1. On the contrary, if Di = Dk, thenSk can be expressed as 0, and Rt can be set depending on the screen condition of the subthreshold leakage-current. Thus, it is necessary to determine the appropriate read-time conditions considering the quality level, test time, and screenability. Note that MSTi of cell i is initialized when the read operation of cell i is activated because of the recharge operation by the sense amplifier. MSTi is also initialized during the periodic refresh operation.

To simulate the MSTi results, we first estimated the stressability of memory cells according to the cell location as explained earlier and derived the mathematical expression in Tables I and II considering the data background and scrambling. Our experiment applies the burst refresh method , which is conducted by a simplified DRAM model consisting of 64 rows and 16 sense amplifiers, for a total of 1024 cells. For easy simulation, the read operation time of the cells is set to 1 μs.



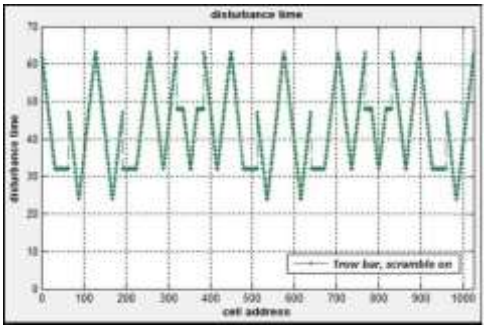


Fig. 5.MSTi simulation results.

(a) MSTi difference according to the data background. (b) MSTi of cell i when refresh time is 112. (c) MSTi of cell with refresh time.

C. Proposed Interleaving Mode

To overcome the variation in MSTi, a new test algorithm is proposed based on the previous model. In the proposed algorithm, an interleaving mode that jumps the word line +2 is used. The algorithm is as follows:

$$\uparrow (wa); \uparrow (ra(t)_{2n}, wa_{2n}); \uparrow (ra);$$

$$\uparrow (ra(t)_{2n+1}, wa_{2n+1}); \uparrow (ra).$$

Instead of the read operation of the sequential address increasing from word line 0 to the end, each read operation of the even word-line cells is activated. All cells are then read to detect the weak cells with the subthreshold leakagecurrent. Each read operation of the odd word line cells is also performed in the same way. Thus, regardless of the cell location, cells on the bit line or bit bar line have stress times that are half of the word line length.

Despite the interleaving mode, MSTi varies because of the refresh conditions. Thus, in order to identify suitable refresh conditions, we simulate the variance of MSTi and the mean of the interleaving mode. The MSTi varies according to the refresh conditions, but there is also no variance in MSTi during the specific refresh time even though the interleaving mode is applied. The mean of the MSTi at that refresh time is higher than at any other refresh time. Thus, a suitable refresh condition can be found to equal the bit-line stress using the interleaving mode as follows:

refresh∝Rt × N/2.

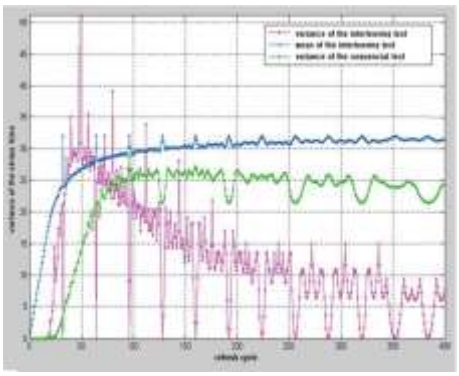


Fig. 6.Variance comparison of MSTi according to the refresh time (solid, scramble on).

As mentioned previously, N is the end of word lines per sense amplifier. Since we use the interleaving mode (+2 word line jump), the equation is divided by 2. This equation means that the variance of MSTi is zero if the refresh operations are conducted immediately after the read operation of the last cell of the column address per sense amplifier.

IV. CONCLUSION

Various screen algorithms have been proposed to detect leakage-current faults. As the length of the gate channel is shortened as down-scaling of the minimum feature size of DRAM, subthresholdleakage-currentfaults havebecomemore serious. Therefore, this paper proposes a new test algorithm to detect and correct subthreshold leakage-current faults. The proposed test algorithm can be used not only to reduce the test time, but also to improve device quality.

REFERENCES

[1] International Technology Roadmap for Semiconductors. (2010) [Online]. Available: http://www.itrs.net/Links/2010ITRS/Home2010.htm

[2] C. Minki, S. Nikhil, R. Arijit, and M. Saibal, "Optimization of burnin test for many-core processors through adaptive spatiotemporal power migration," in Proc. Int. Test Conf., Nov. 2010, pp. 1–9.

[3] A. Pavlov, M. Azimane, J. P. De Gyvez, and M. Sachdev, "Word line pulsing technique for stability fault detection in SRAM cells," in Proc. Int. Test Conf., Nov. 2005, pp. 825–835.

[4] L. Dilillo and B. M. Al-Hashimi, "March CRF:

An efficient test for complex read faults in SRAM memories," in Proc. Design Diag. Electron. Circuits Syst., Apr. 2007, pp. 1–6.

[5] C.-M. Chang, M. C.-T. Chao, H. Rei-Fu, and C. Ding-Yuan, "Testing methodology of embedded DRAMs," in Proc. Int. Test Conf., Oct. 2008, pp. 1–9.

[6] D. Takashima, S. Watanabe, H. Nakano, Y. Oowaki, and K. Ohuchi, "Open/folded bit-line arrangement for ultra-high-density DRAM's," Proc. IEEE J. Solid, State Circuits, vol. 29, no. 4, pp. 539–542, Apr. 1994.

[7] T. Sekiguchi, K. Itoh, T. Takahashi, M. Sugaya, H. Fujisawa, M. Nakamura, K. Kajigaya, and K. Kimura, "A low-impedance open-bitline array for multigigabit DRAM," Proc. IEEE J. Solid, State Circuits, vol. 37, no. 4, pp. 487–498, Apr. 2002.

[8] B. Bhat and F. Mueller, "Making DRAM refresh predictable," in Proc. Real-Time Syst., Euromicro Conf., Jul. 2010, pp. 145–154.