TEST PATTERN AND POWER MINIATURIZATION USING FAULT INJECTION METHOD FOR DIAGNOSING SCAN CHAIN FAILURES

BHARATHI.S

II Year M.E Student, Department of ECE,

Dhanalakshmi Srinivasan College of Engineering, Anna University

Coimbatore, Tamilnadu, India.

Bharathibe455@gmail.com

THANGAMANI .M

Assistant Professor, Department of ECE,

Dhanalakshmi Srinivasan College of Engineering, Anna University.

Coimbatore, Tamilnadu, India.

thangamani1712@gmail.com

ABSTRACT:

During the testing of chip, diagnosing chain failure is most important. Multiple faults in the scan chain can be diagnosed using the selective triggering method for the reduction of transitions in the scan cell. This triggering technique reduces switching activity in the circuit under test and increases the clock frequency of the scanning process. A reordering is utilized in this system to avoid the large number of transitions. By the process of reordering area may increase and the number of test patterns used for testing also increased. Reduce the test pattern count and area by adding fault injection technique in the system. Once the fault type is identified

the subsequent fault injection process can be more realistic and thus lead to test pattern reduction at the result. This reduces the power and area than the preceding method.

IndexTerms— Chain failures, fault detection, fault injection, reordering, test pattern count.

I. INTRODUCTION

Integrated circuits are much easier to design and manufacture and are more reliable using VLSI. Due to reduced size and low power consumption, manufacturing cost is also reduced. For testing modern digital circuits DFT techniques is used. DFT techniques are required to improve the quality and reduce the test cost of the digital circuit, simplifying the test, debug and diagnose tasks. During the circuit testing faults can be diagnosed. A fault simulator approaches the target faults in a circuit, to detect which type of faults is detected by a given set of test vectors. Fault simulation time increases for fault detection analysis because there are many faults to approach. The selected storage elements are connected into a single or multiple chains are called scan chain. Scan design performs this operation by superseding all the selected storage elements with scan cells. It has one additional SI port and SO port. One or more scan chains are created by connecting the SO port as a SI port of the next scan cell. A fault is the state which affects the output of the tested circuit .The circuits can be tested by applying the n inputs and its m outputs, by comparing it with the output of a fault-free circuit. Pattern which is applied as an input is called test vector. In [1] the diagnosis is based on a single stuck-at fault model. The modeled single faults in a scan chain may affect either an input of a latch along the scan path or output of a latch along both scan and functional paths. This strategy presented a pattern generation algorithm and demonstrated the practicality of our approach by illustrating that run times are within acceptable limits. In this [2] work, for identifying single stuck-at faults in scan paths a diagnostic methodology is used. In case of multiple faults these scheme always identifies the

fault closest to the scan-out pin. A symbolic fault simulation is used in an efficient scan chain diagnosis method to achieve high diagnostic resolution and list for one or more defects in scan chains. The main ideas of the scan chain diagnosis method are twofold with the symbolic simulation responses: 1) analysis for the reduction of the candidate scan cells and 2) using the backward tracing method the final candidate scan cells can be identified. Scan chain diagnosis starts with a flush test applications. It can detect the fault type and location only as briefly explained in [4], [5]. To generate the test patterns ATPG tools can be used in the compression architecture [6].

Several techniques are used to diagnose faults, its type and to identify the exact location of the faults in the circuit path. Some of them used to detect single faults in multiple chain and multiple faults in single chain only [5], [9], [10]. Due to this the test time and the cost for manufacturing the IC can be increased .Both test data compression and test response compaction can be used to reduce time and cost. In this MISRs are using to reduce both time and space where as XOR gates reduces only space. During the process of testing the circuit by applying the test patterns, X's (do not care) present in the patterns and the whole output will affects in the compactors. To handle these problems the solution are described in [6], [8], [11], [14]. An simple way to secure the essential patterns for a chain is to mask the other remaining chains for a specific patterns. AND based masking circuitry is utilized for masking the Xs and prevents them from reaching the space compactors [12]. If for a pattern, response is observed in only one scan chain in each output channel, while all the other chains are masked, it is called 1-hot pattern. The procedure to diagnose scan chain is more difficult because when a circuit fails the flush test, not all patterns are applied. Only subsets of patterns are applied and the observed are responses are used to diagnose the faulty chains. Accordingly, we have proposed a tester architecture that use the

pattern which has detailed information for testing. The pattern may cancel each other if simultaneous failures occur in the two or more scan chains. Due to this problem the whole process will takes time to complete the testing. To reduce the test pattern count and power consumption, fault injection technique is used. The transition methodology [18] achieves test power reductions by adding the gates in between the scan cells. These [7] scan architecture uses a triggering chain in addition to the data registers. Retaining data causes a small number of transitions at the data register outputs and lowers the power dissipation.

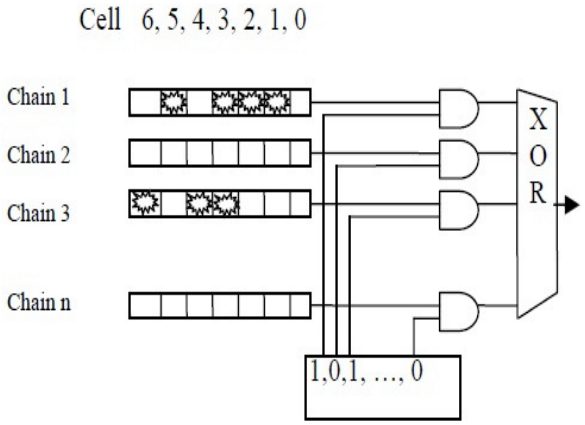


Fig.1. Multiple faults at scan chain

In the paper [3] explains the multiple fault diagnosis method. When multiple chains fail due to the presence of multiple faults, diagnosis becomes even more difficult. For scan chains, we have considered at most two faults because the fault pair, consisting of a fault close to the scan-in and other fault close to the scan-out, will dominate the remaining faults. For example, fig 1, the scan cell 1, 2, 3 and 5 are the 4 failing bits in the scan chain ‘1’. Other than these chains ‘3’ also has the failing bits in the scan cell 3, 4, 6. The chain selection logic selects the masking values for the signals are shown in the figure 1. Both the failing chains 1 and 3 are to inspect through the space

compactor with single output. There are 5 failing bits at scan cell 1, 2, 4, 5 and scan cell 6 after the space compactor due to compaction. It is difficult for the diagnosing tool to determine which scan chain is causing the failing bits. If two failing bits occurs at the same scan shift cycle for the two failed chains may cancel each other, which also makes the chain diagnosis difficult. Due to these problems the whole process will takes time to complete the testing. When we are using the above methods to detect the faults in the circuit maximum number of test patterns has to be used.

The sections which are remained in the paper can be explained below: In section II the preceding work of this paper has been reviewed. The flow of test pattern generation can be described in section III. The propound work has been detailed in section IV. And section V, VI consists of conclusion and future work.

II.PRECEDING WORK

The multiple fault diagnosis method uses the repetition in fault detection by the test patterns applied to the chain and that will select and apply the patterns which have detailed information for diagnosis. Then the control signal will check the mask signal and the indicated failed chain to decide whether apply or skip the current pattern. This leads to increase the time and power to complete the testing. To avoid this problem selective triggering technique is used in the tester architecture. This [7], [19] technique decreases the changing state in the testing circuit and increases the clock frequency of the scanning process. A chain reordering is utilized in this architecture to avoid the large number of transitions. This reduces the power consumption during testing. For this system, flow diagram can be explained in fig 2.

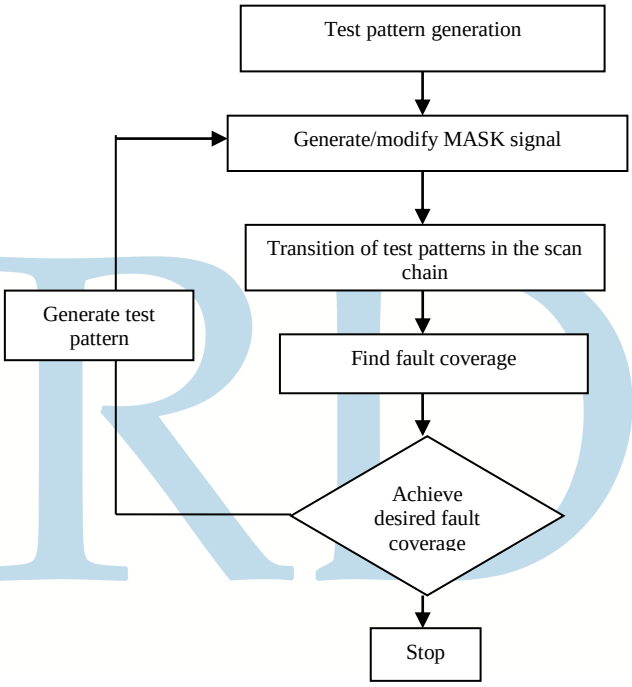


Fig 2.Flow diagram for test generation

The design process has been explained in the test generation flow pattern fig 2. These patterns are generally applied from the top of the pattern list. First, the test patterns can be generated and tested the patterns by applying to all the chains. These test patterns contain faults as X's. After that, generated test pattern will be masked by applying masking method to prevent the output of the chain from the faulty output. Generating some essential patterns for any failed scan chain combinations in the masking method. However, masking arbitrary scan chains will lower fault coverage. Therefore, mask generation scheme should minimize pattern count as well. Then the

transition is performed in the scan chain. For the transition process, selective triggering technique is used to reorder the cells in the scan chains. The operation of selective triggering technique [7] can be explained as shown in the figure 3.

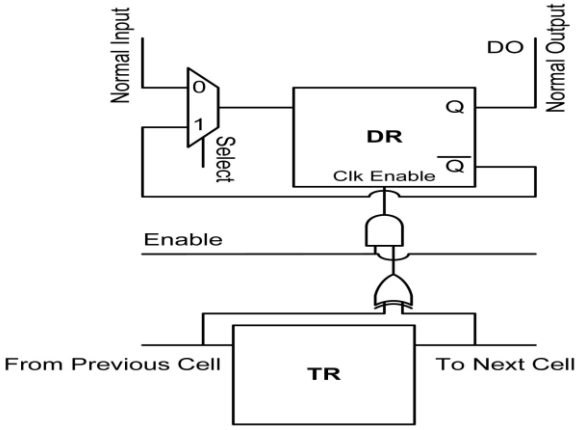


Fig 3. Selective triggering architecture

It contains DR and TR flip flop for the reordering of the cells. The TR chain provides the data required for selective triggering. The Enable signal is high (active) and the multiplexer selects the input connected to the Q output of DR flip-flops. The value of DR flip-flop remains unchanged, if the XOR output is '0' and it is inverted when the output is '1'. The values which are stored in the DR flip flop cause an inversion due to the output '1' at the XOR of a cell in the trigger mode. After the reordering of scan cells in the chain, it has to decide whether it achieves fault coverage or not. If the fault is detected then the process will be stopped. Test pattern count can be increased during the generation of mask signals. The increased test pattern consumes power and time to complete the process. This is due to the process of CUT takes time to compare the observed and obtained results. This approach is the drawback of this system.

To overcome these problems new technique has been introduced in the proposed method. When these patterns are used according to the proposed multiple fault diagnosis methodology, then only the results are close to the optimum value. The first one is the generalized diagnosis

algorithm for multiple fault diagnosis in a single chain. Here, for each applied pattern, the algorithm injects all possible single as well as double faults in the chain and finds the compacted responses. The observed responses are then compared with these responses and a ranking of the faults are given based on the matching. For both the techniques, number of faults in a chain is unknown.

III.PROPOUND WORK

During the testing of chip, diagnosing chain failure is most important. Multiple faults in th e scan chain can be diagnosed using the selective triggering method for the reduction of transitions in the scan cell. This triggering technique reduces switching activity in the circuit under test and increases the clock frequency of the scanning process. A reordering is utilized in this system to avoid the large number of transitions. By the process of reordering area may increase and the number of test patterns used for testing also increased. Reduce the test pattern count and area by adding fault injection technique in the system. Once the fault type is identified the subsequent fault injection process can be more realistic and thus lead to test pattern reduction at the result. This reduces the power and area then the preceding method.

2.1 Fault Injection Method

A physical defect or imperfection that occurs within some of the hardware or software components is called fault. The technique which is very important for the estimation of design parameters such as reliability, safety and fault coverage. It includes the system by inserting the faults in it and monitoring the system to determine its behavior in response to the fault. When executed, a fault may cause an error, which is an invalid state in the system. It has two types of techniques, 1) simulator commands and 2) VHDL code modification. Simulator commands techniques modify the values and itys timing model signals and variables without altering the

VHDL code. The number of fault models which are injected in this technique is lesser than the other techniques. In the VHDL code modification technique, the original VHDL code is modified by either inserting saboteurs [20], [21] or mutating the components of the model. In this work, VHDL code modification is used. A saboteur is a special VHDL component added to the original model [21]. The task assigned to this component is to make different in its value or the timing characteristics of the signals to give the occurrence of a fault. During the normal operation of the system, the component remains inactive. Thus, this technique is only used to the structural descriptions. A mutant method is used to replace the original component or gates with the alternative component or gate. It works like the original component in a inactive mode otherwise it behaves like the component in presence of faults.

There are three ways for mutation,

- Adding saboteurs to the structural model description
- Structural descriptions can be modified by replacing the sub components (ex. AND gate can be replaced by OR gate)
- By modifying Syntactical structures of behavior descriptions.

2.2 Flow diagram of modified tester method

The inject-and-evaluate paradigm can also be applied to scan chain diagnosis with a specific fault model. Unlike the hardware-assisted method, this is a software method without any area overhead. As noted previously, the flush test, although ineffective for fault location, can be used for classifying the fault type first. Once the fault type is known, the subsequent fault injection process can be more realistic and thus lead to a more accurate result. A diagnostic test procedure of this type operates the same as normal scan testing, which goes through a scan–capture–scan scenario for each test vector as shown in fig 4.

1. Run a flush test to guess the type of the faults by injecting the faulty test pattern.
2. Pick one possible fault candidate. Inject the fault effect into the scan chain.
3. Mask signals are generated in the memory for the test patterns.
4. Compare the failing vector with the fault-free vector. Accumulate the matching score for each fault candidate and determine the fault coverage.
5. If it achieves the fault coverage the process will stop otherwise the process will continue until it achieves desired fault coverage.

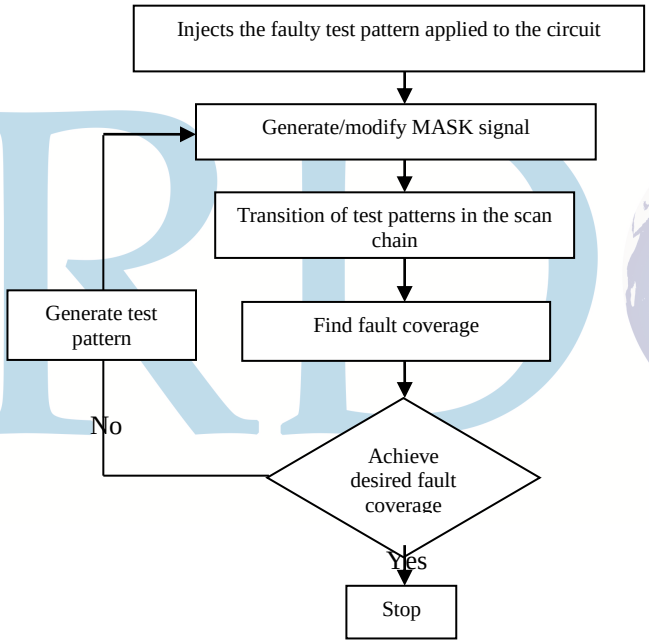


Fig 4.Flow diagram of Proposed modified test generation

3.3 Proposed Tester Architecture

The scan chain diagnosis procedure is even more difficult when a circuit fails the flush test instead of the entire test set only a few test patterns are applied. These patterns are generally applied from the top of the pattern list. The applied patterns might not have enough information to diagnose the scan chains. Since our masking scheme works on the entire pattern set, the policy

of applying only first few patterns in conventional tester would result in poor performance of the suggested strategy. In the following, we propose simple tester architecture is shown in the fig 5 to implement our scheme. The following are the components of the tester.

1) Flush Pattern Memory: In this flush patterns are stored. Flush pattern are used to detect the fault types and its location in the scan cells.

2) Inject the faulty test pattern: Test patterns are stored in it. Test pattern are already generated depends on the faults injected to the circuit by applying the faults in the test pattern.

3) Mask Signal Memory: The mask signals corresponding to each pattern are stored. Mask signals are also necessary for flush patterns.

4) Scan chain register: It contains the flush pattern from the memory.

5) Selective triggering architecture: Triggering chain decides where a data flip-flop must toggle or retain its old value.

6)Response Memory: Compacted responses are stored in it. It also has a comparator that compares the circuit under test (CUT) response with the golden response and generates Pass/Fail signal.

7) Failed Chain Index Memory: It contains the indices of the scan chains failing flush test.

8) Control Logic: The control logic checks the mask signal and the failed chain indices to decide whether to apply or skip the current pattern.

The whole process can be applied to the any one of the benchmark circuits to check the circuit design. In this we are using s298 benchmark circuit to analyze the output variations for the faulty and fault free test pattern.

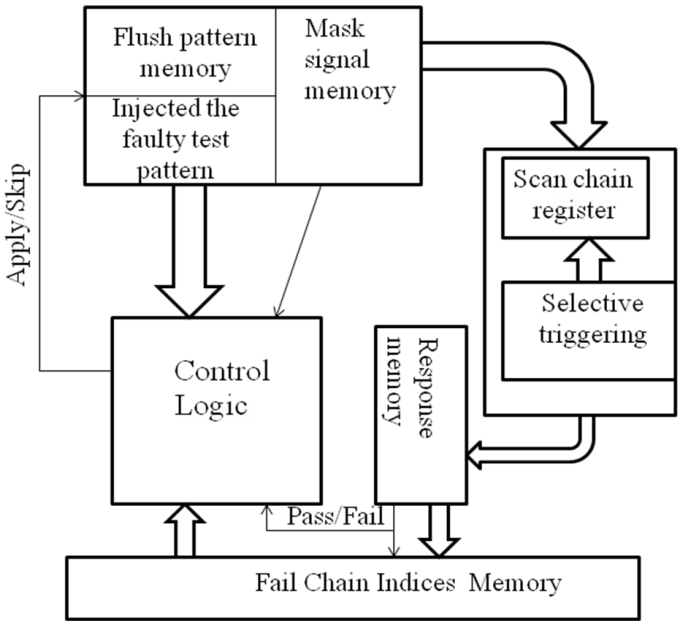


Fig 5. Block diagram of the tester architecture

Compared with the conventional external tester, the modified tester contains a control logic that decides whether to apply or skip a pattern. The rest of the tester architecture remains unaltered. For the proposed modified architecture, we have actually implemented two different approaches to select which of the patterns are going to be applied. In the first approach, the test patterns are selected on the fly. For a pattern next in the list, the tester generates a signal, apply/skip based on whether the pattern contains enough information for diagnosis. The applied pattern count reaches a specified limit, the tester stops. The advantages of this approach are that the control logic for the tester is fairly simple and also the test time is less. The control logic of this approach can easily be generated by calculating the number of unmasked failed chains for a particular pattern.

IV.EXPERIMENTAL RESULT

4.1. Modelsim Output Waveform:

The scan chain diagnosis process with fault injection technique can be executed. The system is executed using the modelsim. During the execution of the scan chain masking process the output can be obtained at various time. It does not takes much time to complete the execution. It shows the generation of fault injected test pattern which detects the faults and the variation of faulty and fault free output in fig 6 and 7.

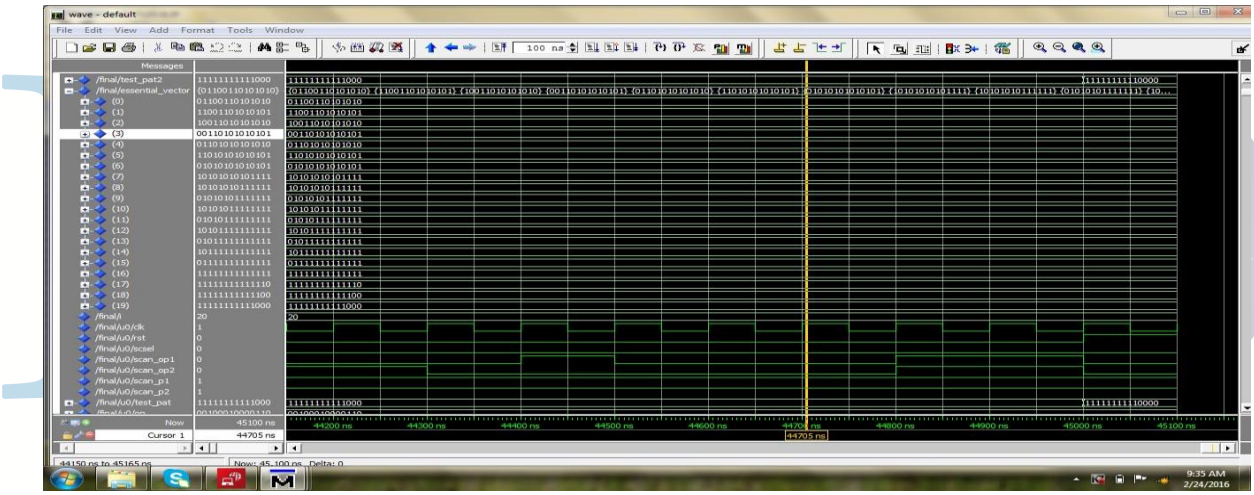


Fig 6. Waveform represents the generation of fault injected test vectors

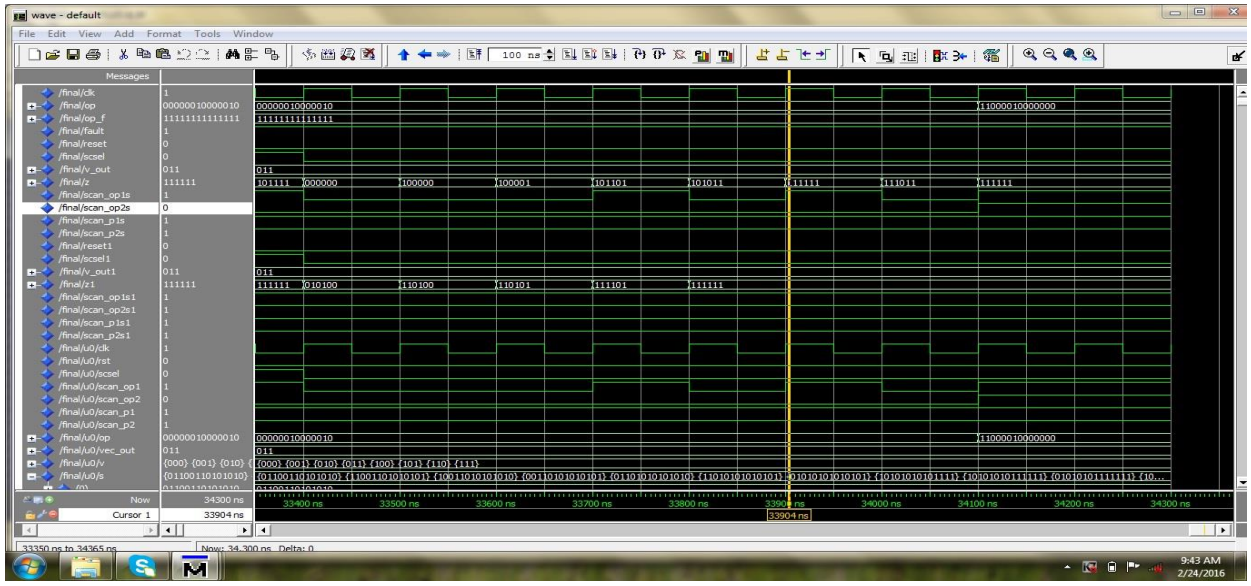
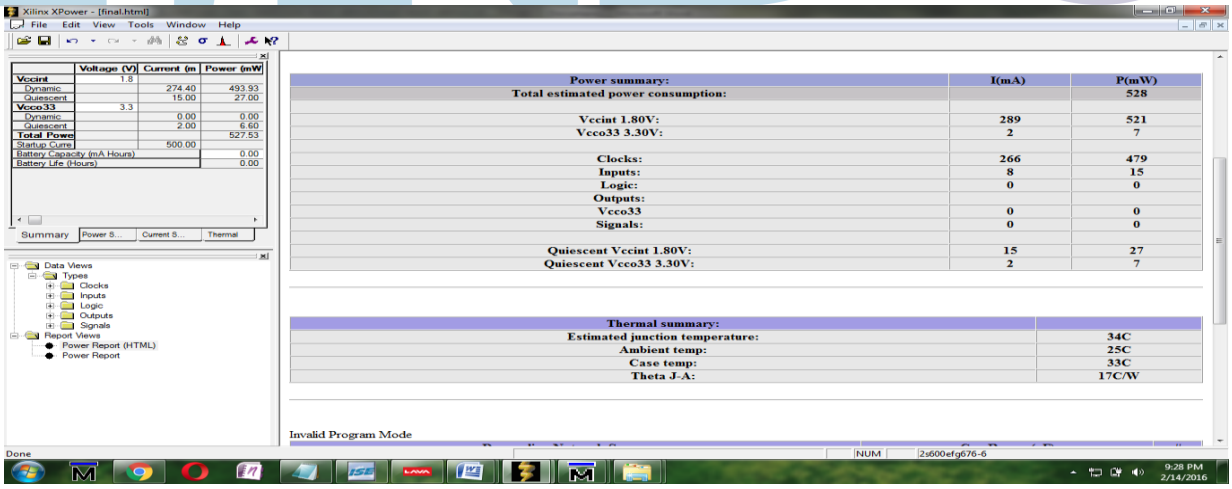


Fig 7. Waveform for the faulty and fault free output using fault injection technique

4.2 Xilinx Output

In these output shows the total power required to complete the scan chain faults Detection.

The consumption of power and area to complete the process is shown in Fig 8 and Fig 9.



Power summary:	I(mA)	P(mW)
Total estimated power consumption:		528
Vccint 1.80V:	289	521
Vcco33 3.30V:	2	7
Clocks:	266	479
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Thermal summary:	
Estimated junction temperature:	34C
Ambient temp:	25C
Case temp:	33C
Theta J-A:	17C/W

Fig 8.power consumption for the propound work

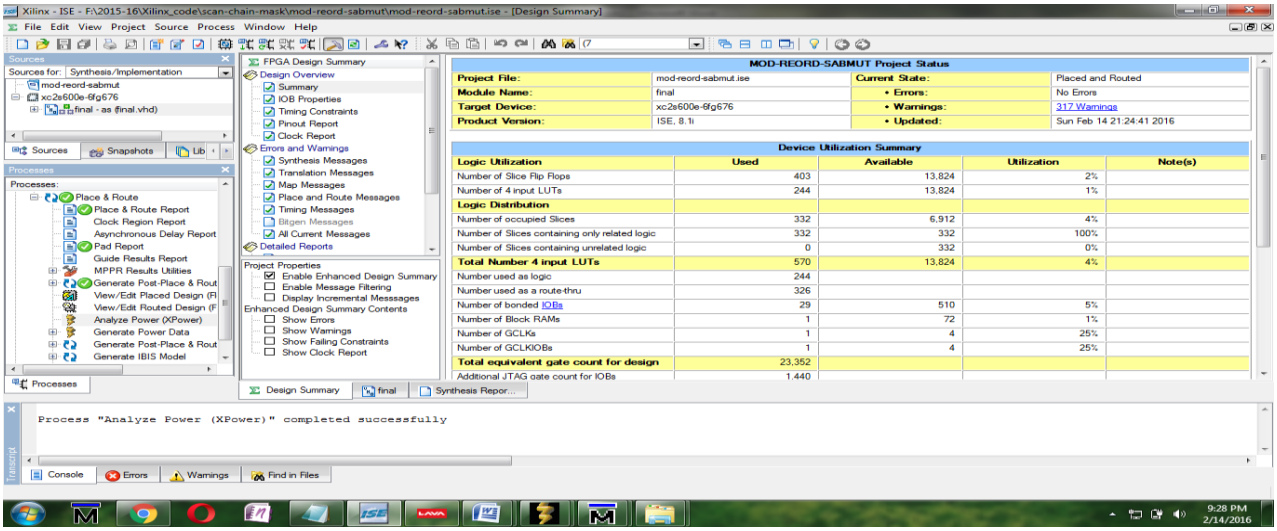


Fig 9. Area for diagnosing chain failures using fault injection technique

V.CONCLUSION

The scan chain diagnosis technique is used to diagnose multiple chain failures in response compaction environment. The multiple fault diagnosis technique encodes some information along with the test patterns, which can be used for diagnosis of scan chains. New tester architecture with fault injection techniques is designed to reduce the number of test patterns used for testing. It will select and apply only those patterns having enough information for diagnosis. At end of the testing area can be reduced up to 40-45% compare to the previous method.

References

[1] Sandip Kundu, "Diagnosing Scan Chain Faults," IEEE Transactions on VLSI Systems, Vol. 2, No. 4, Dec 1994 Pp. 512-526.

[2] Samantha Edirisooriy, Geetan dirisooriya, "Diagnosis of Scan Path Failures," IEEE Motorola Computer Group 1995,pp - 250-251.

[3] Subhadip Kundu, Santanu Chattopadhyay, Indranil Sengupta, And Rohit Kapur, "Scan Chain Masking For Diagnosis Of Multiple Chain Failures In A Space Compaction Environment", In Proc IEEE Trans. On VLSI Systems, Vol. 23, No. 7, July 2015

[4] Sunghoon Chun And Alex Orailoglu "Disc: A New Diagnosis Method For Multiple Scan Chain Failures" In Proc IEEE Trans. On Comp.Aided Design Of IC And Systems, Vol. 29, No. 12, December 2010

[5] Ruifeng Guo Yu Huang Wu-Tung Cheng Mentor Graphics Corp. Wilsonville, "A Complete Test Set To Diagnose Scan Chain Failures" In Proc IEEE Int. Test Conf ., 2007.

[6] Anshuman Chandra And Rohit Kapur , "Interval Based X-Masking For Scan Compression Architectures" In Proc IEEE Int. Symp. On Quality Electronic Design ,2008 .

[7] Mohammad Hosseinabady, Shervin Sharifi, Fabrizio Lombardi, And Zainalabedin Navabi, "A Selective Trigger Scan Architecture For Vlsi Testing" , In Proc IEEE Trans.On Comp., Vol. 57, No. 3, March 2008.

[8] Wu-Tung Cheng And Yu Huang , "Enhance Profiling-Based Scan Chain Diagnosis By Pattern Masking" In Proc IEEE Asian Test Symposium, 2010.

[9] Ruifeng Guo And Srikanth Venkataraman "An Algorithmic Technique For Diagnosis Of Faulty Scan Chains" In Proc. IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 25, No. 9, September 2006.

[10] Yu-Long Kao, Wei-Shun Chuang, And James C.-M. Li "Jump Simulation: A Technique For Fast And Precise Scan Chain Fault Diagnosis" In Proc IEEE International Test Conference, 2006 .

[11] Vivek Chickermane, Brian Foutz, And Brion Keller, "Channel Masking Synthesis For Efficient On-Chip Test Compression", In Proc. IEEE Itc Int. Test Conf., 2004.

[12] Xun Tang, Ruifeng Guo, Wu-Tung Cheng, Sudhakar M. Reddy, "Improving Compressed Test Pattern Generation For Multiple Scan Chain Failure Diagnosis",In Proc. Design Autom.Test Eur.Conf.Exhibit.,Apr.2009.

[13] K. Stanley, "High-accuracy flush-and-scan software diagnostic," *IEEEDesign Test Comput.*, vol. 18, no. 6, pp. 56–62, Nov./Dec. 2001.

[14] A. Chandra, Y. Kanzawa, and R. Kapur, "Proactive management of X's in scan chains for compression," in *Proc. 10th Int. Symp. Qual.Electron. Design*, Mar. 2009, pp. 260–265.

[15] Y. Huang, W.-T. Cheng, R. Guo, T.-P. Tai, F.-M. Kuo, and Y.-S. Chen,"Scan chain diagnosis by adaptive signal profiling with manufacturing ATPG patterns," in *Proc. Asian Test Symp.*, Nov. 2009, pp. 35–40.

[16] S. Narayanan and A. Das, "An efficient scheme to diagnose scan chains," in *Proc. Int. Test Conf.*, Nov. 1997, pp. 704–713.

[17] C.Kalamani, Dr. K.Paramasivam, "Survey of Low Power Testing Using Compression Techniques," IJECT Vol. 4, Issue 4, Oct - Dec 2013.

[18] Juan-Carlos Baraza, Joaquín Gracia, Sara Blanc, Daniel Gil, and Pedro-J. Gil, "Enhancement of Fault Injection Techniques Based on the Modification of VHDL Code" IEEE trans on VLSI Systems, Vol. 16, No. 6, June 2008.

[19] Seongmoon Wang, and Sandeep K. Gupta, "An Automatic Test Pattern Generator for Minimizing Switching Activity During Scan Testing Activity," IEEE Ttransactions on computer-aided design of integrated circuits and systems, vol. 21, no. 8, august 200,pp- 954-968.

[20] E. Jenn, J. Arlat, M. Rimén, J. Ohlsson, and J. Karlsson, "Fault injection into VHDL models: The MEFISTO tool," in *Proc. FTCS*, 1994, pp.356–363.

[21] J. Boué, P. Pétillon, and Y. Crouzet, "MEFISTO-L: A VHDL-based fault injection tool for the experimental assessment of fault tolerance,"in *Proc. FTCS*, 1998, pp. 168–173.